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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Applicant Number	Unknown
Filing Date	Even Date Herewith
First Named Inventor	Gu, Shuo
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 1 of 1

Attorney Docket No: MA-108

**US PATENT DOCUMENTS**

Examiner Initial *	Cite No	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date if Appropriate
GP	A1	5,821,152	10/13/1998	Han et al.			
GP	A2	5,923,968	07/13/1999	Yamazaki et al.			
GP	A3	6,146,966	11/14/2000	Hirota et al.			
GP	A4	6,204,156	03/20/2001	Ping			
GP	A5	US20020028541A1	03/07/2002	Lee et al.			

**FOREIGN PATENT DOCUMENTS**

Examiner Initials *	Cite No	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>
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**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials *	Cite No *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
GP	A6	BANERJEE, ADITI., et al. , "Fabrication and Performance of Selective HSG Storage Cells for 256 Mb and 1Gb DRAM Applications", <u>IEEE Transactions on Electron Devices</u> , Vol.47, No.3, (3/2000),584-592	
GP	A7	BO, XIANG-ZHENG., et al. , "Spatially selective single-grain silicon films induced by hydrogen plasma seeding", <u>J. Vac. Sci. Technol. B</u> 20(3), (May/Jun 2002),	
GP	A8	DAHLHEIMER, C..E. , et al. , "Laser-Interference Crystallization of Amorphous Silicon", 54-55	
GP	A9	OH, CHANG-HO., et al. , "A Proposed Single Grain-Boundary Thin-Film Transistor", <u>IEEE Electron Device Letters</u> , Vol.22, No.1, (1/01),20-22	
GP	A10	SONG, I.H. , et al. , "A New Multi-Channel Dual-Gate Poly-Si TFT Employing Excimer Laser Annealing Recrystallization on pre-patterned a-Si thin Film", <u>0-7803-7463-X02 (C) 2002 IEEE</u> , (2002),	
GP	A11	SUBRAMANIAN, VIVEK., et al. , "Controlled Two-Step Solid-Phase Crystallization for High-Performance Polysilicon TFTs", <u>IEEE Electron Device Letters</u> Volume: 18 Issue: 8, Aug 1997, (1997),378 -381	
GP	A12	YAMAUCHI, N., et al. , "Polycrystalline silicon thin films processed with silicon ion implantation and subsequent solid-phase crystallization: Theory, experiments, and thin-film transistor applications", <u>Journal of Applied Physics</u> , vol. 75, (1994),3235-3257	

EXAMINER

DATE CONSIDERED

90/3/05

Substitute Disclosure Statement Form (PTO-1449)

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. \* Applicant's unique citation designation number (optional) \* Applicant is to place a check mark here if English language Translation is attached